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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/640,856	08/13/2003	Paige M. Holm	CML01045CR	9182

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MOTOROLA, INC.
CORPORATE LAW DEPARTMENT - #56-238
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PHOENIX, AZ 85018

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/640,856	HOLM ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,642,076 to Yaung et al.

Regarding claim 1, Yaung et al. (figures 3-7) teach a electronic imaging component, the component comprising:

an electronics layer (a sensor diode in the substrate) (column 3, lines 30-32);

a photosensing element (a photodiode, 116), the photosensing element fabricated in a vertically integrated optically active layer (a portion of layer 114);

a substantially vertical interconnect (194);

the photosensing element (116) further comprising a junction (a portion of p-n diode) surrounding and at least partially encompassing the vertical interconnect (a portion of 194), wherein charge carriers may be substantially laterally drawn toward the axis of at least one of the junction and the interconnect; and

the optically active layer (a portion of layer 114) positionally disposed proximate to a metalization surface of the electronics layer (a sensor diode in the substrate).

Yaung et al. differ from the claimed invention by not showing the optically active layer bonded to the electronics layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the optically active layer bonded to the electronics layer, since the bonding method is a known method for forming layers.

Regarding claim 2, Yaung et al. teach the electronics layer is substantially fully processed.

Regarding claim 3, Yaung et al. teach the photosensing element comprises a photodiode (116).

Regarding claim 4, Yaung et al. teach the optically active layer comprises of Si (silicon layer, 114).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,642,076 to Yaung et al. in view of US Patent No. 6,509,636 to Tsai et al.

The disclosures of Yaung et al. are discussed as applied to claims 1-4 above.

Regarding claim 5, Yaung et al. differ from the claimed invention by not showing the bonding comprises of die-to-wafer bonding. However, Tsai et al. teach the CMOS image sensor chip, which is bonded to the substrate (20) (column 1, lines 16-19; column 3, lines 27-32). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsai et al. into the device taught by Yaung et al. because it holds the chip in place. The combined device shows the bonding comprises of die-to-wafer bonding.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,642,076 to Yaung et al. in view of US Patent No. 6,344,669 to Pan.

The disclosures of Yaung et al. are discussed as applied to claims 1-4 above.

Regarding claim 6, Yaung et al. differ from the claimed invention by not showing interconnect extends substantially through the optically active layer. However, Pan (figures 2A-I) teaches interconnect comprises metallized via (71), and extends substantially through the optically active layer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Pan into the device taught by Yaung et al. because it provides interconnection between the device and the external element. The combined device shows interconnect extends substantially through the optically active layer.

5. Claims 7-13, 15, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,642,076 to Yaung et al. in view of US Patent No. 6,611,013 to Rhodes.

Regarding claim 7, the disclosures of Yaung et al. are discussed as applied to claims 1-4 above.

Yaung et al. differ from the claimed invention by not showing a photosensing element array and a plurality of substantially vertical interconnects. However, Rhodes (figure 17) teaches a plurality of substantially vertical interconnects (382) and a photodiode array (column 1, lines 17-20; column 2, lines 4-17). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Rhodes into the device taught by Yaung et al. because it provides more interconnections between the device and the external element. The combined device shows a photosensing element array, a plurality of

substantially vertical interconnects, the photosensing element array further comprising a plurality of junctions substantially surrounding and at least partially encompassing the plurality of vertical interconnects, wherein charge carriers may be substantially laterally drawn toward the axis of at least one of the plurality of junctions and the plurality of interconnects, the optically active layer bonded to the electronics array layer, and the optically active layer positionally disposed proximate to a metalization surface of the electronics array layer.

Regarding claim 8, the combined device shows an electronic imaging having a relatively high interconnect density.

Regarding claim 9, Yaung et al. and Rhodes differ from the claimed invention by not showing the high interconnect density comprises about one connection per up to about 10-250 square microns. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the high interconnect density comprises about one connection per up to about 10-250 square microns, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 10, the combined device shows the interconnects comprise a plurality of at least one of metallized vias.

Regarding claim 11, Yaung et al. and Rhodes differ from the claimed invention by not showing the photosensing element fill factor is up to about 75%. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the photosensing element fill factor is up to about 75%, since it has been held that discovering an optimum value

of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 12, Yaung et al. and Rhodes differ from the claimed invention by not showing the photosensing element fill factor is greater than 75%. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the photosensing element fill factor is greater than 75%, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 13, Yaung et al. and Rhodes differ from the claimed invention by not showing the photosensing element fill factor is up to about 100%. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the photosensing element fill factor is up to about 100%, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 15, the combined device shows a plurality of vertically integrated optically active layers.

Regarding claim 16, the combined device shows a plurality of vertically integrated electronic processing layers.

Regarding claim 17, the combined device shows the optically active layer comprises of Si.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yaung et al. in view of Rhodes, and further in view of US Patent No. 6,366,317 to Mattison et al.

The disclosures of Yaung et al. and Rhodes are discussed as applied to claims 7-13 and 15-17 above.

Regarding claim 14, Yaung et al. and Rhodes differ from the claimed invention by not showing the electronics circuitry is optimized for substantial parallel processing of array-captured images. However, Mattison et al. teach the CMOS image sensor is optimized for substantial parallel processing of array-captured images (column 4, lines 62-64; column 7, lines 43-58). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Mattison et al. into the device taught by Yaung et al. and Rhodes because it provides better operation of the device. The combined device shows the electronics circuitry is optimized for substantial parallel processing of array-captured images.

7. Claims 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yaung et al. in view of Rhodes, and further in view of US Patent No. 6,683,646 to Hosier et al.

Regarding claim 18, the disclosures of Yaung et al. and Rhodes are discussed as applied to claim 7 above.

Yaung et al. and Rhodes differ from the claimed invention by not showing a plurality of photosensing element. However, Hosier et al. teach a plurality of photodiodes (photosensing element) (abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hosier et al. into the device taught by Yaung et al. and Rhodes because it receives more image for device. The combined

device shows a plurality of photosensing element arrays, the photosensing element arrays fabricated in a plurality of vertically integrated optically active layers.

Regarding claim 20, the combined device shows the optically active layers comprise at least one of Si.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yaung et al. and Rhodes in view of Hosier et al., and further in view of US Patent No. 6,498,336 to Tian et al.

Regarding claim 19, the disclosures of Yaung et al., Rhodes and Hosier et al. are discussed as applied to claims 18 and 20 above.

The combined device differs from the claimed invention by not showing different optically active layers are suitably adapted to demonstrate sensitivity to different regions of the electromagnetic spectrum. However, Tian et al. teach image sensors can be implemented for regions of the electromagnetic spectrum (column 5, lines 15-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tian et al. into the device taught by Yaung et al., Rhodes and Hosier et al. because it provides better performable of the device. The combined device shows different optically active layers are suitably adapted to demonstrate sensitivity to different regions of the electromagnetic spectrum.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
September 3, 2004

Sara W Crane
Sara Crane
Primary Examiner